JULIEN ROCHE

Security Project Manager & Technical Director

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PROFESSIONAL EXPERIENCE

XDIGIT | MEYREUIL, FRANCE

Security Project Manager & Technical Team Lead | November 2024 - Present

- Leading and managing secure product development projects, supervising all phases from design to implementation
- Developing strategic security technology roadmaps aligned with business objectives and market trends
- Driving innovation initiatives resulting in improved product security and competitive advantage
- Collaborating with executive management to align security requirements with business strategy
- Managing cross-functional relationships with sales teams to provide technical leadership during pre-sales and post-delivery phases
- Supervising security evaluations and strategic cost estimates for client projects

Key Achievement: Secure X-Band Receiver Project

- Led the project management of a secure X-band receiver development with strict security requirements
- Managed the security aspects of SAR ADC converters in 22FDX Global Foundries technology
- Implemented security risk mitigation strategies for high-speed sampling requirements
- Coordinated cross-functional teams to deliver a solution meeting security specifications
- Balanced security requirements with power consumption and performance constraints

CORTUS SAS | MEYREUIL, FRANCE

Manager, Custom Cells Design Team | June 2021 - November 2024

- Led the custom cells design team with a focus on secure component development for advanced European multicore systems
- Spearheaded the analog design and implementation of the clock system, including the full custom Phase-Locked Loop (PLL) architecture, ensuring robust, low-jitter, and high-precision clock distribution critical for multicore RISC-V processors
- Managed cross-functional technical initiatives, collaborating closely with European partners as part of the eProcessor project, to align PLL specifications and integration with broader system requirements
- Oversaw the analog-digital interface and clock-tree interactions, optimizing phase noise, skew, and synchronization across multiple processing cores and system domains
- Implemented project management methodologies to address complex security and reliability challenges in clock system design for secure SoCs
- Established and enforced security governance frameworks and best practices for all phases of analog and mixed-signal design and development

Key Achievement: Variable Frequency PLL for European Processor Project

- Led the development of a variable frequency PLL for a European processor project
- Coordinated teams across multiple companies and countries, serving as the primary technical liaison
- Managed relationships with partners from Germany, France, and the Netherlands
- Resolved technical challenges to achieve a wide frequency range while maintaining phase noise performance
- Delivered a solution that became a key component in the processor architecture, enabling flexible clock management
- Implemented design methodologies and team coordination to meet project timelines

WISEKEY SEMICONDUCTORS (NOW SEALSQ) | MEYREUIL, FRANCE

Analog Design Engineer, later promoted to Custom Cells Design Team Manager | September 2016 - June 2021

- Directed RF transceiver design in 0.13um/55nm for Type A and Type B communication on the ISO14443 protocol

- Collaborated with executive management on strategic initiatives related to security solutions for IoT applications and smart cards
- Progressed from an individual contributor role to a team management role
- Led the Secured Analog Mixed-Signal, Power Management, and Non-Volatile Memory team in the IoT IC design group
- Represented the company as a member of the AFNOR certification group for ISO14443 and ISO15693 RF communication standards
- Developed and implemented security technology roadmaps aligned with emerging threats and market opportunities

INSIDE SECURE | MEYREUIL, FRANCE

Ph.D. Analog Design Engineer | October 2010 - September 2016

- Provided technical leadership and design methodology support to internal designers
- Designed critical security components, including DCDC and communication interfaces (SWP, I2C, GPIO)
- Contributed to strategic technology planning for security solutions
- Designed analog components: contact/contactless interfaces, frequency cells, etc.

ATMEL CORPORATION - SMART CARD BUSINESS UNIT

Ph.D. Microelectronic Engineer | November 2008 - February 2011

- Worked in the Smart Card Business Unit on secure microcontroller design
- Provided in-depth dedicated design methodology support to internal designers
- Deployed and used microelectronic design tools and flows in a broad range of areas
- Verified and implemented digital, analog, and mixed-signal ASICs
- Performed semiconductor device modeling with technological CAD

Analog Designer and Ph.D. Student | November 2004 - November 2008

- Designed robust devices with USB specification for smart card applications in the Smart Card BU
- Worked on doctoral thesis in parallel with professional responsibilities
- Developed low-power and secure analog circuits for smart card applications

STMICROELECTRONICS

ST Designer | January 2004 - September 2004

- Final study internship on timing delay modeling in digital design
- Extended the logical effort model to propagation delay
- Modeled propagation delays of different gates (MathCAD)
- Simulated with Cadence and extracted net model with StarRCXT
- Analyzed crosstalk and modeled the inductive impact of nets

ORGANIZATIONS & ENGAGEMENTS

CHERI Alliance

CHERI Alliance Ambassador | May 2025 - Present

As a CHERI Ambassador, I promote a technology that represents a major advance in security by addressing the root causes of memory safety vulnerabilities. Unlike traditional software-based protections, CHERI (Capability Hardware Enhanced RISC Instructions) integrates fine-grained memory protection and compartmentalization directly into hardware, enforcing bounds and permissions at the pointer level. This hardware-enforced approach drastically reduces risks from common exploits such as buffer overflows and use-after-free errors, which account for nearly 70% of all software vulnerabilities. https://cheri-alliance.org/

EDUCATION & CERTIFICATIONS

UNIVERSITÉ AIX-MARSEILLE | Ph.D. IN MICROELECTRONICS | 2005-2008

Thesis: "Design of Robust, Low-Power, and Low-Cost Devices with USB Specification for Smart Card Applications"

Research focused on developing innovative circuit designs for USB interfaces in smart card applications, with emphasis on power efficiency, cost optimization, and robust performance across various conditions.

Activities and tools:

- State of the art (PLL, DLL, P/PLL...)
- System studies (mathCAD, ADS)

- Phase noise analysis
- Design flow:
  - Design of each block of the solution (charge pump, VCO, voltage-controlled current source, low-noise frequency multiplier, phase-frequency detector, low-noise and high-precision comparator, loop filter, low-noise regulator)
  - Testing process, power, and temperature impact
  - Layout and test chip design
  - Post-layout simulations
  - On-chip probe measurements

POLYTECH MONTPELLIER | MASTER OF SCIENCE IN MICROELECTRONICS | 2001-2004

GOOGLE | FOUNDATIONS OF PROJECT MANAGEMENT | Issued Feb 2025

Credential ID: 71GBBFUP00PG

PATENTS & PUBLICATIONS

- A 50MHz Phase Locked Loop with Adaptive Bandwidth for Jitter Reduction - IEEE-ICM (2007)
- A Differential 3.3V BICMOS Buffer with Current Consumption and Linearity Control for RF Mixer - IEEE-ICM (2007)
- A Low Noise Fast-Settling Phase Locked Loop with Loop Bandwidth Enhancement - IEEE-NEWCAS and TAISA (2008)
- A New Adaptation Scheme For Low Noise and Fast Settling Phase Locked Loop - IEEE Midwest Symposium on Circuit and Systems (2008)
- A Phase Locked Loop with Loop Bandwidth Enhancement for Low-Noise and Fast-Settling Clock Recovery - IEEE International Conference on Electronics, Circuits, and Systems (2008)

TECHNICAL EXPERTISE

- **Security Project Management:** Leading secure product development lifecycles, risk assessment, and security certification processes
- **Analog Security Protection:** Power supply monitors, glitch detection, frequency monitors, temperature sensors for EAL 5+ certified products
- **Secure Elements:** TRNG (True Random Number Generator) design, VFO, analog components for Common Criteria EAL5+ certified Secure Elements
- **RF Communication:** ISO14443 and ISO15693 standards (AFNOR certification group member), RF transceiver design for banking applications (Visa and MasterCard certified)
- **Analog Design:** Low-noise analog filters, low-jitter and high-speed PLL design, secured PADs (IO, CLK, Rst, GPIO, I2C, SPI)
- **Power Management:** Secure power regulation, power consumption masking for side-channel attack prevention
- **Design Tools:** Cadence/Synopsys IC design environment
- **Languages:** French (Native), English (Professional), German (Basic)

EXECUTIVE LEADERSHIP

- **Project Management:** Leading complex technical projects from conception to delivery with focus on security requirements
- **Strategic Vision:** Developing and executing technology roadmaps aligned with business goals
- **Executive Communication:** Effectively communicating complex technical concepts to various stakeholders

- **Team Leadership:** Building, mentoring, and leading high-performing engineering teams
- **Certification Management:** Managing certification processes (Common Criteria, EMVCo, FIPS)
- **Business Acumen:** Understanding market dynamics and translating technical capabilities into business value
- **Innovation Management:** Fostering a culture of innovation and continuous improvement
- **Risk Management:** Identifying and mitigating technical and security risks in product development